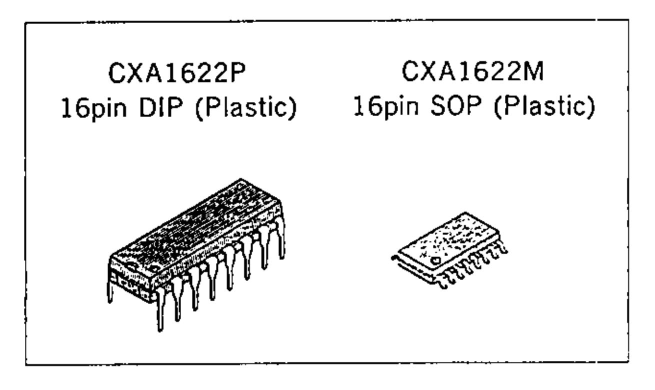
SONY # CXA1622P/M

Stereo Power Amplifier/Monaural BTL Power Amplifier

Description
The CXA1622P/M is a bipolar IC developed as power amplifier for compact radio cassettes with built-in pre-amplifier and power amplifier electrical volume.

Features
- Use one channel in stereo mode
  - EIAJ output=450 mW (Typ.), V_{CC}=6 V, R_L=8 Ω (CXA1622P)
  - EIAJ output=110 mW (Typ.), V_{CC}=3 V, R_L=8 Ω (CXA1622M)
- BTL mode
  - EIAJ output=360 mW (Typ.), V_{CC}=3 V, R_L=8 Ω (CXA1622P)
  - EIAJ output=320 mW (Typ.), V_{CC}=3 V, R_L=8 Ω (CXA1622M)
- Built-in electrical volume
- Built-in ripple filter (ripple rejection 34.5 dB typ.)
- Selection between stereo power amplifier and monaural BTL power amplifier is possible by switching Pin 2.

Applications
Suitable for audio power amplifier for stereo and monaural radios and power amplifier for radio cassette and walkman.



Structure
Bipolar silicon monolithic IC

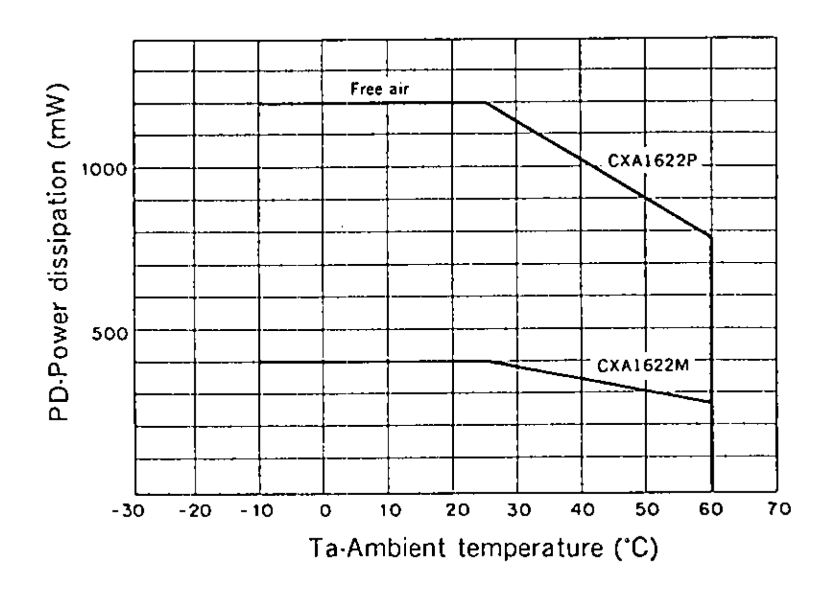
Absolute Maximum Ratings (Ta=25 °C)

• Supply voltage	V_{CC}	8	V
• Operating temperature	T_{opr}	−10 to +60	°C
• Storage temperature	T_{stg}	−65 to +150	°C
• Allowable power dissipation	P_D	1200 (CXA1622P) 410 (CXA1622M)	mW mW

Operating Conditions (Ta=25 °C)
Supply voltage

Stereo mode	1.8V to 7.0V (CXA1622P) 1.8V to 4.5V (CXA1622M)
Monaural BTL mode	1.8V to 4.5V (3V recommended)

Power dissipation curve CXA1622P/M



E92121A26-HP

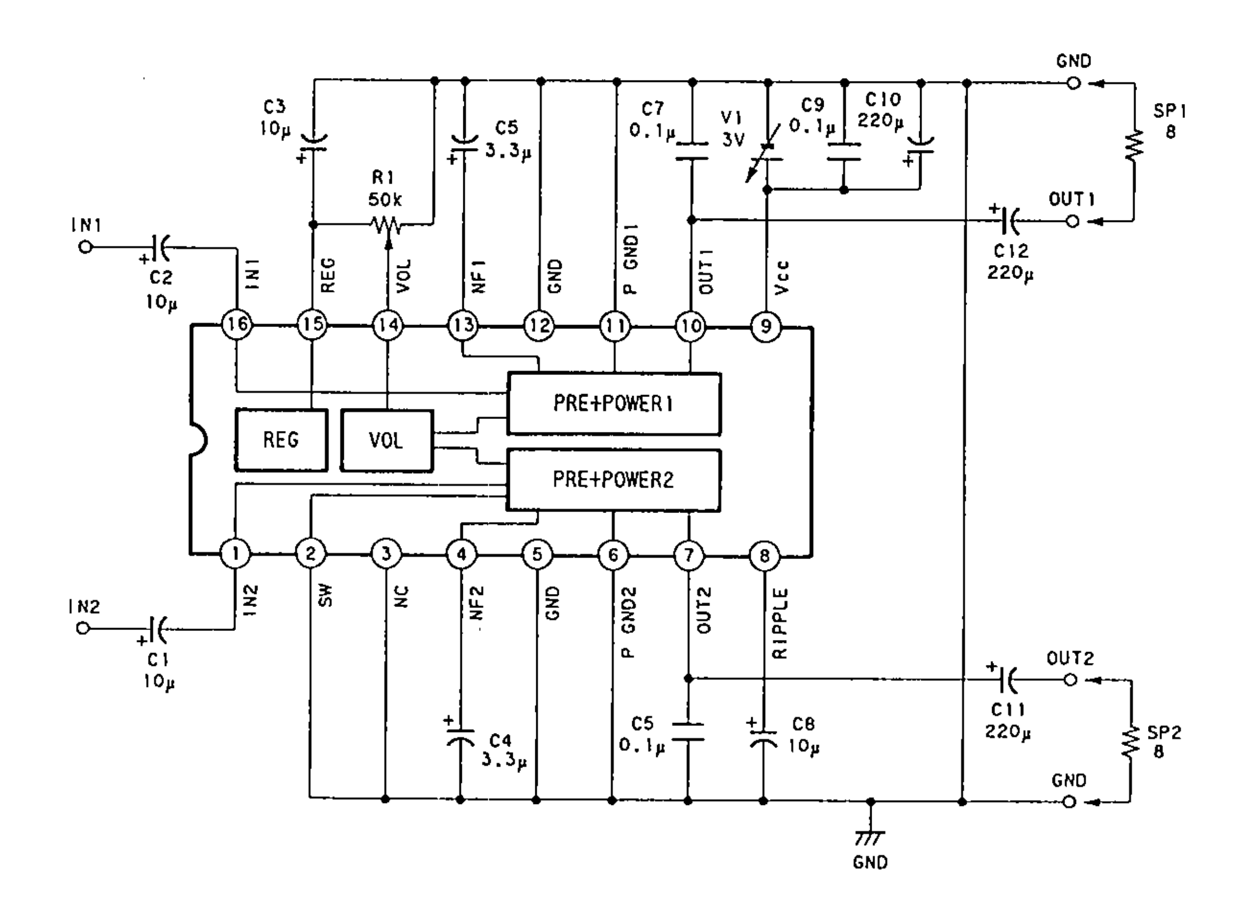
Pin Description

Pin No.	Symbol	Equivalent circuit	Pin voltage		Description
			3V	6V	
1, 16	IN1 IN2		0	0	Input
3	NC		—	—	
4, 13	NF1 NF2		1.5	3	Power amplifier NF. Connected to time constant 4.7 μF.
5, 12	CND1 CND2		0	0	Pre-amplifier GND
6, 11	P-GND1 P-GND2		0	0	Power amplifier GND
7, 10	OUT1 OUT2		1.5	3	Power amplifier output
8	RIPPLE		2.72	5.43	Connected to time constant 10 μF for ripple filter.
9	V_{CC}		3	6	V_{CC}
14	VOL		0 to 1.25	0 to 1.25	Control gain with change in voltage (0 to 1.25 V) to electrical volume control pin

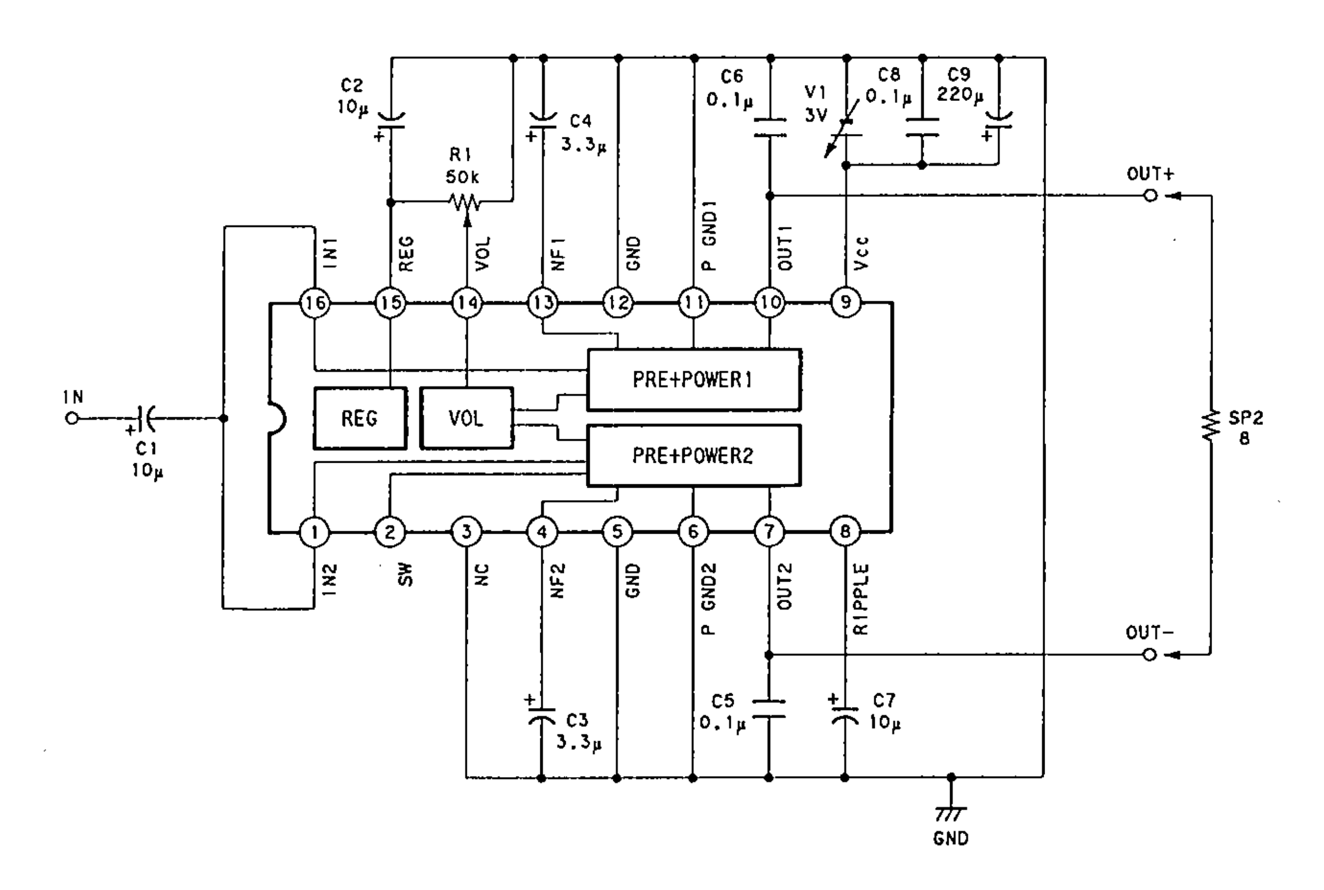
Pin No.	Symbol	Equivalent circuit	Pin voltage		Description
			3V	6V	
15	REG		1.25	1.25	Regulator pin
2	SW		1.25	1.25	Mode selection SW • BTL mode when open • Stereo mode when connected to GND

Block Diagram, Pin Configuration, and Application Circuit

1) Stereo mode



2) BTL mode



* The input signal enters the pre-amplifier with attenuation controlled with DC at Pin 14 and then it is amplified by the approximately 30 dB (fixed) power amplifier.
* The state of Pin 2 can be used to select between stereo mode and monaural BTL mode.
  The pre-power 1 and pre-power 2 output are positive phase output when Pin 2 is GND. Pre-power 2 is inverse output of pre-power 1 output when Pin 2 is open.

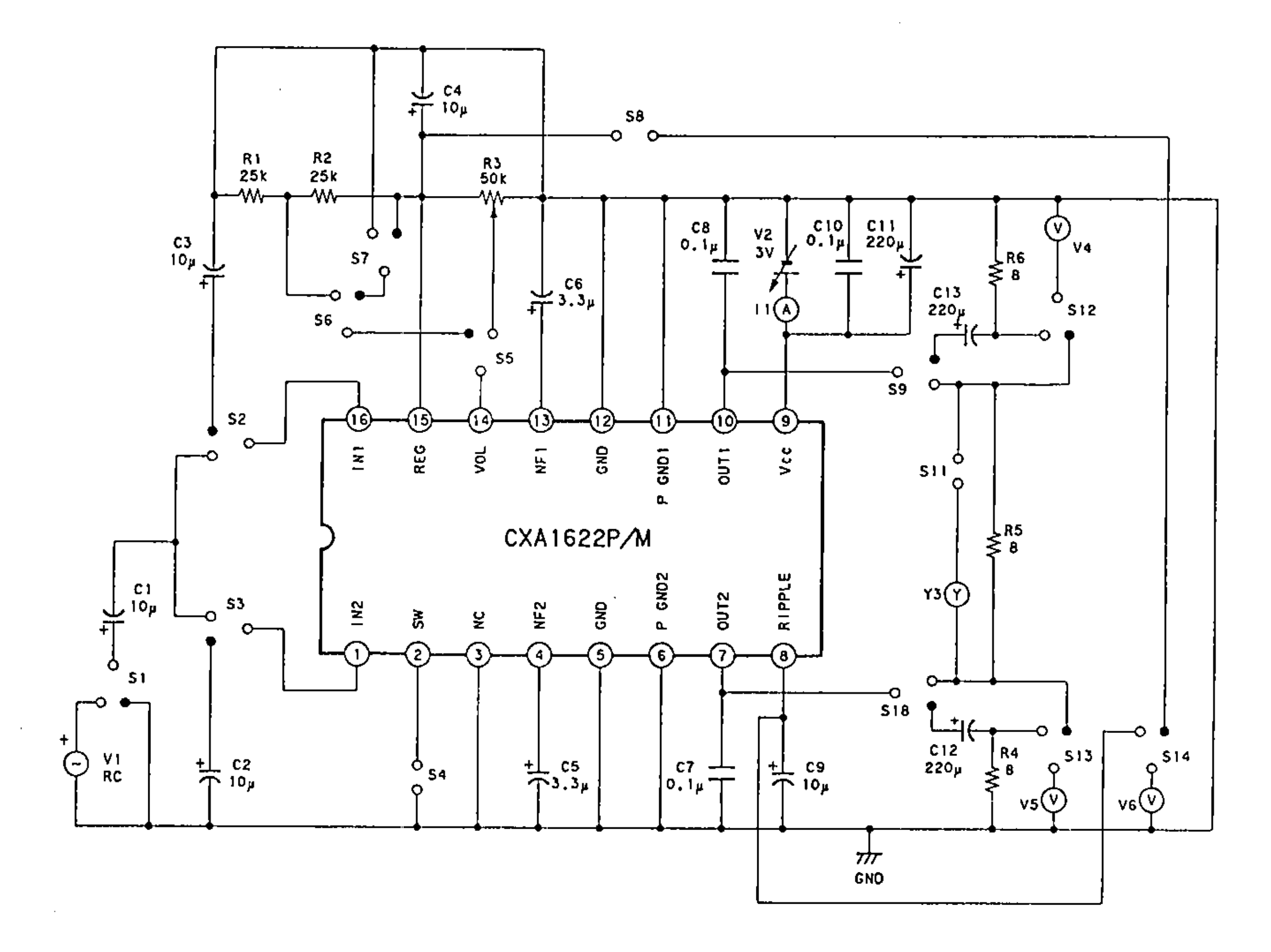
Stereo mode { Upper : CXA1622P (Vcc=6V) / Lower : CXA1622M (Vcc=3V) }

Function block	TEST No.	Test item	BIAS SW Conditions S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	Input point	Input waveform and Bias description	Test point	Output waveform and Description of test method	Min.	Typ.	Max.	Unit
Typical conditions for each bias																								
	1	Circuit current during no signal	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF			I_1	Circuit current during no signal	1.0 1.0	3.0 3.0	8.2 7.7	mA
	2	Audio voltage gain Lch	ON	ON	OFF									ON					V_4	V_1 = −40 dBm 1kHz	28 27	33.7 32.6	38 36	dB
	3	Audio voltage gain Rch		OFF	ON									OFF	ON				V_5	V_1 = −40 dBm 1kHz	28 27	33.7 32.6	38 36	dB
	4	Channel balance																	V_4, V_5	L and R channel balance	−3	0	−3	dB
	5	Attenuation Lch		ON	OFF			ON						ON	OFF				V_4	V_1 = −40 dBm 1kHz Output level difference between max volume and half volume	1.5 1.0	5.8 4.3	12 12	dB
	6	Attenuation Rch		OFF	ON									OFF	ON				V_5	V_1 = −40 dBm 1kHz Output level difference between max volume and half volume	1.5 1.0	5.8 4.3	12 12	dB
	7	EIAJ output Lch		ON	OFF		ON							ON	OFF				V_4	V_1 = −20 dBm 1kHz, RL=8Ω Output level where THD=10 %	350 90	450 110		mW
	8	EIAJ output Rch		OFF	ON									OFF	ON				V_5	V_1 = −20 dBm 1kHz, RL=8Ω Output level where THD=10 %	350 90	450 110		mW
	9	Audio distortion factor Lch		ON	OFF									ON	OFF				V_4	V_1 = −20 dBm 1kHz, RL=8Ω Distortion factor when output is 50 mW		0.7	2.5	%
	10	Audio distortion factor Rch		ON	OFF									OFF	ON				V_5	V_1 = −20 dBm 1kHz, RL=8Ω Distortion factor when output is 50 mW		0.7	2.5	%
	11	Residual noise level Lch	OFF	OFF	OFF		OFF	OFF						ON	OFF				V_4	Noise level during no signal at max volume		−65	−60	dBm
	12	Residual noise level Rch												OFF	ON				V_5	Noise level during no signal at max volume		−65	−60	dBm
	13	Crosstalk L → R	ON	ON																V_1 = −40 dBm 1kHz Rch output level when Lch is input		−60	−56	dBm
	14	Crosstalk R → L		OFF	ON									ON	OFF					V_1 = −40 dBm 1kHz Lch output level when Rch is input		−60	−56	dBm

BTL mode $V_{CC}=3$ V Upper : CXA1622P
Lower : CXA1622M

Function block	TEST No.	Test item	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	Input point	Input waveform and Bias description	Test point	Output waveform and Description of test method	Min.	Typ.	Max.	Unit
Typical conditions for each bias																								
	1	Circuit current during no signal	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	OFF	ON	ON	OFF			I_1	Circuit current during no signal		3	7	mA
	2	OUTPUT DC bias lag											ON						$\lvert V_3 \rvert$	Output DC bias lag		0	30	mV
	3	Audio voltage gain	ON																V_3	$V_1=-40$ dBm 1 kHz	34 30	38 37	42 43	dB
	4	Attenuation						ON											V_3	$V_1=-40$ dBm 1 kHz Output level difference between max volume and half volume	1.5 1.0	6.0 5.0	12 12	dB
	5	EIAJ output					ON												V_3	$V_i=-20$ dBm 1 kHz, RL=8Ω Output level where THD=10 %	260 220	360 320		mW
	6	Audio distortion factor																	V_3	$V_1=-20$ dBm 1 kHz, RL=8Ω Distortion factor when output is 50 mW		1.0	2.5	%
	7	Residual noise level					OFF	OFF											V_3	Noise level during no signal at max volume		−65	−62	dBm

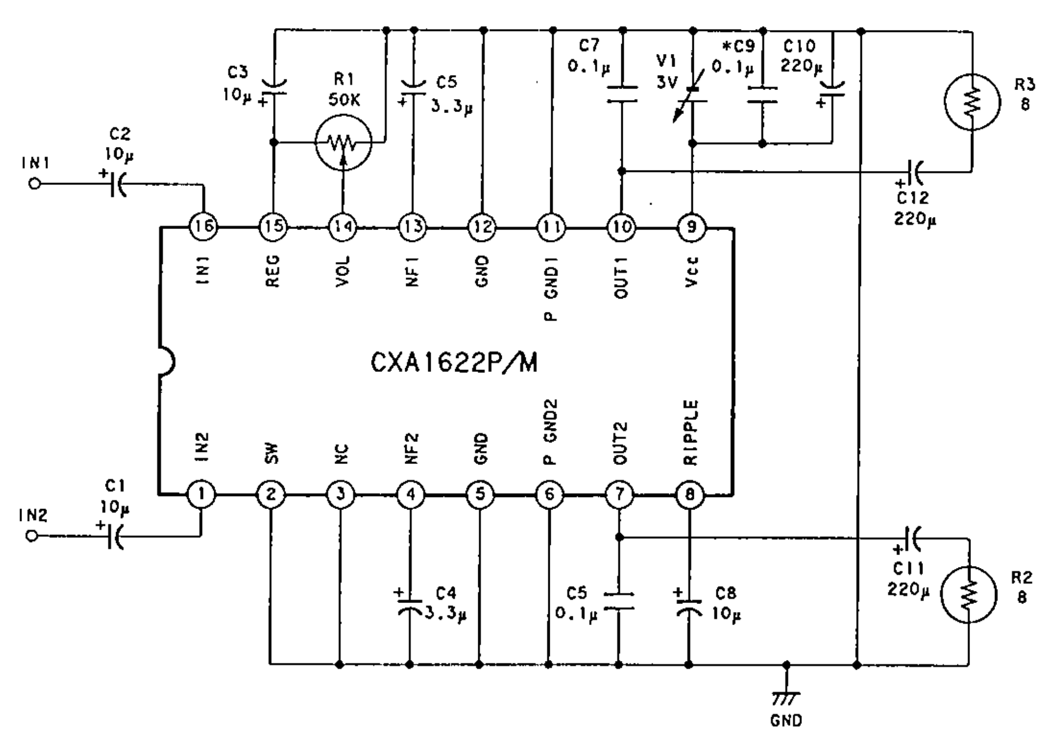
Electrical Characteristics Test Circuit



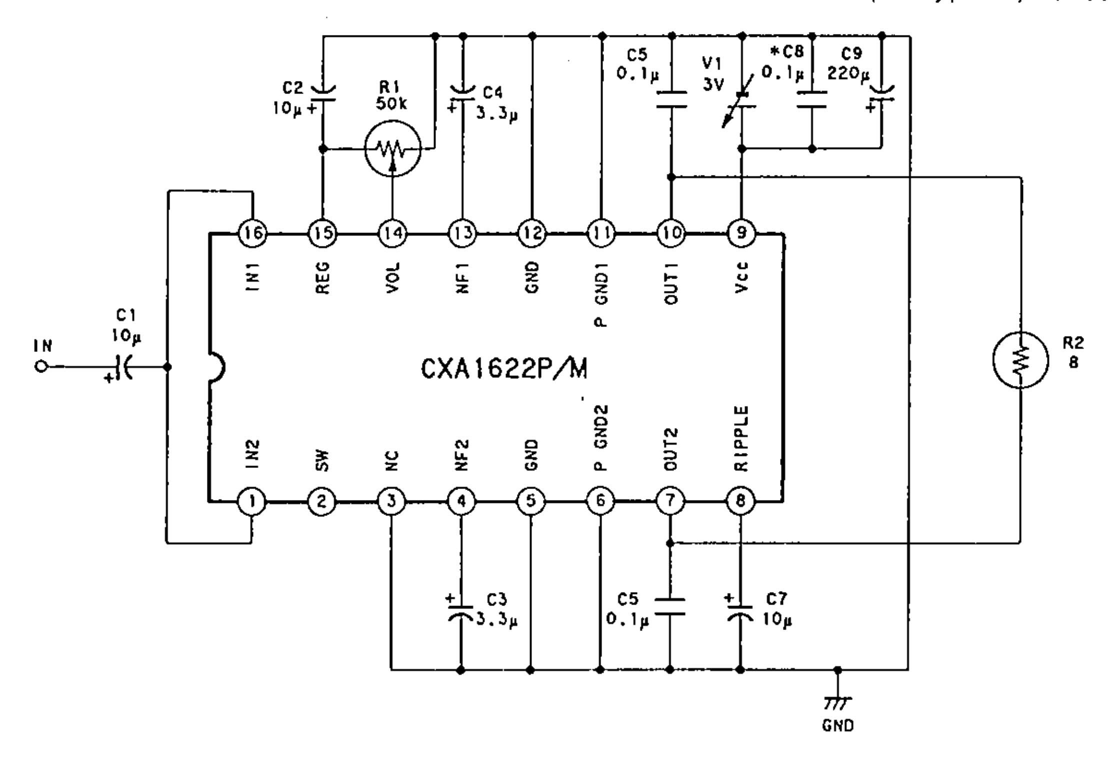
Notes on Operation

- Set print pattern to low impedance because Pins 6 and 11 are GND of power amplifier output stage.
- The value of the phase correction capacitance attached to Pins 7 and 10 varies slightly according to the print pattern.
- Provide a large land for DIP type Pin 5 because it also serves as heat dissipation pin.
- Place the by-pass capacitor of V_{CC} (Pin 9)as close to the pin as possible.

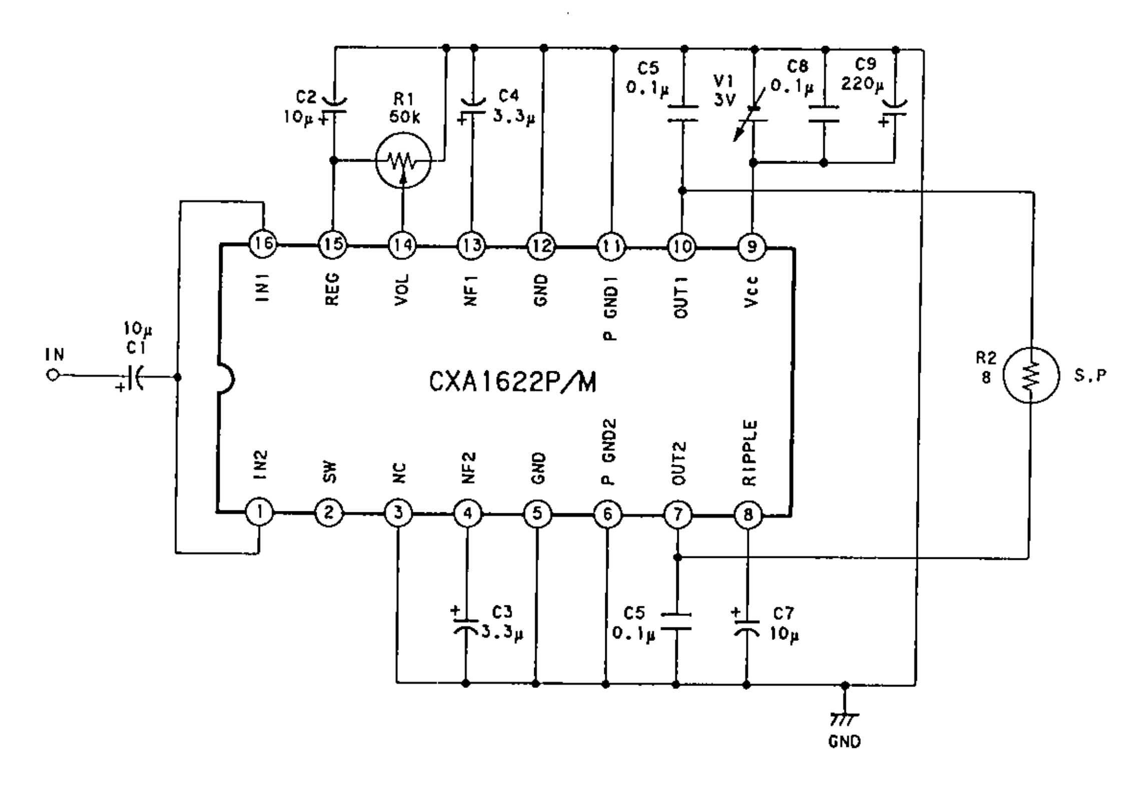
Stereo output single mode



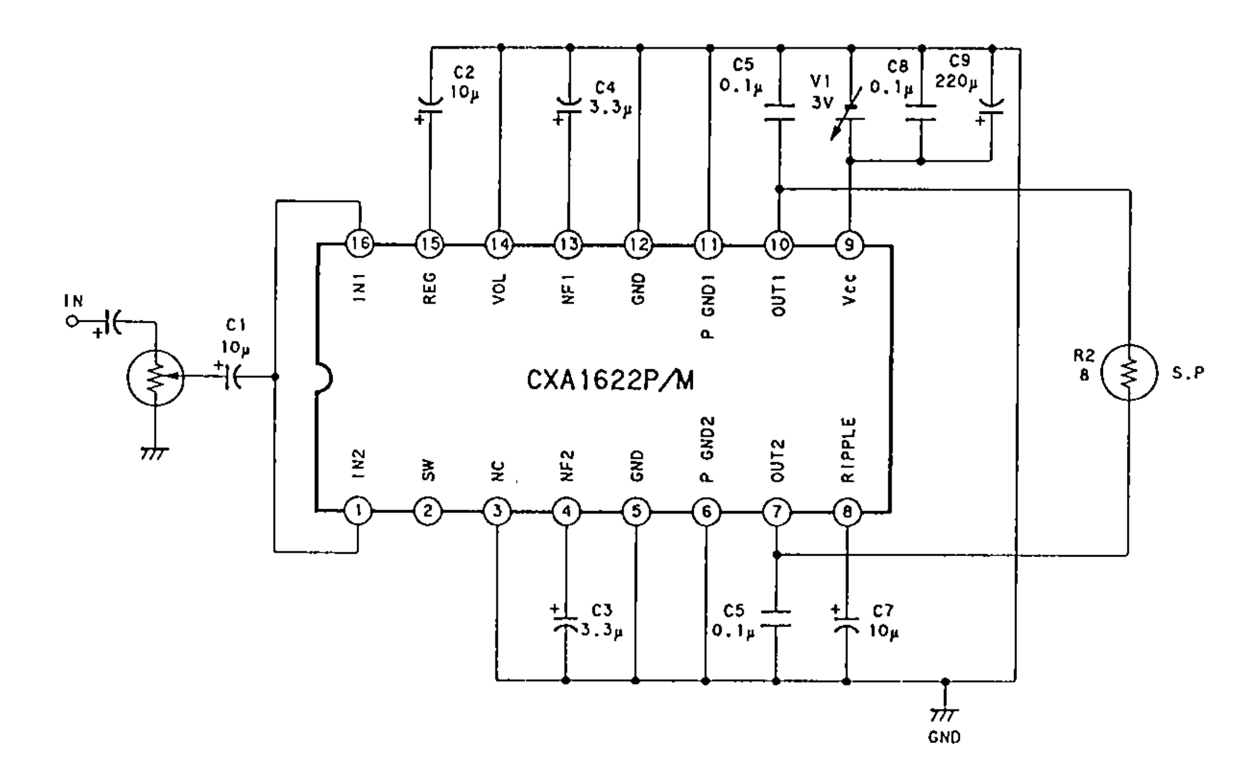
Monaural output BTL mode



When using internal IC electrical volume in BTL mode

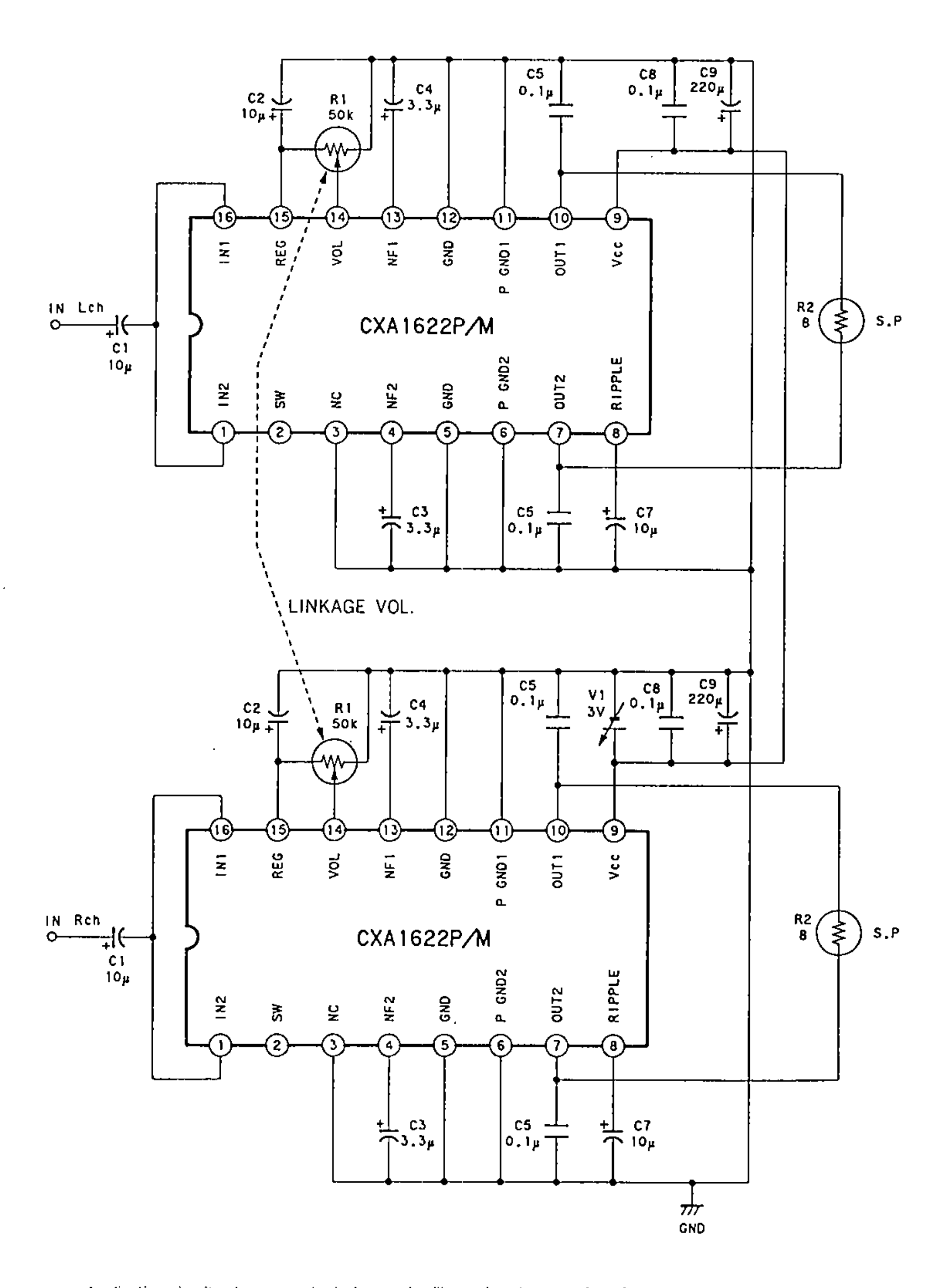


When using IC as fixed gain amplifier in BTL mode



BTL, Stereo Application Circuit

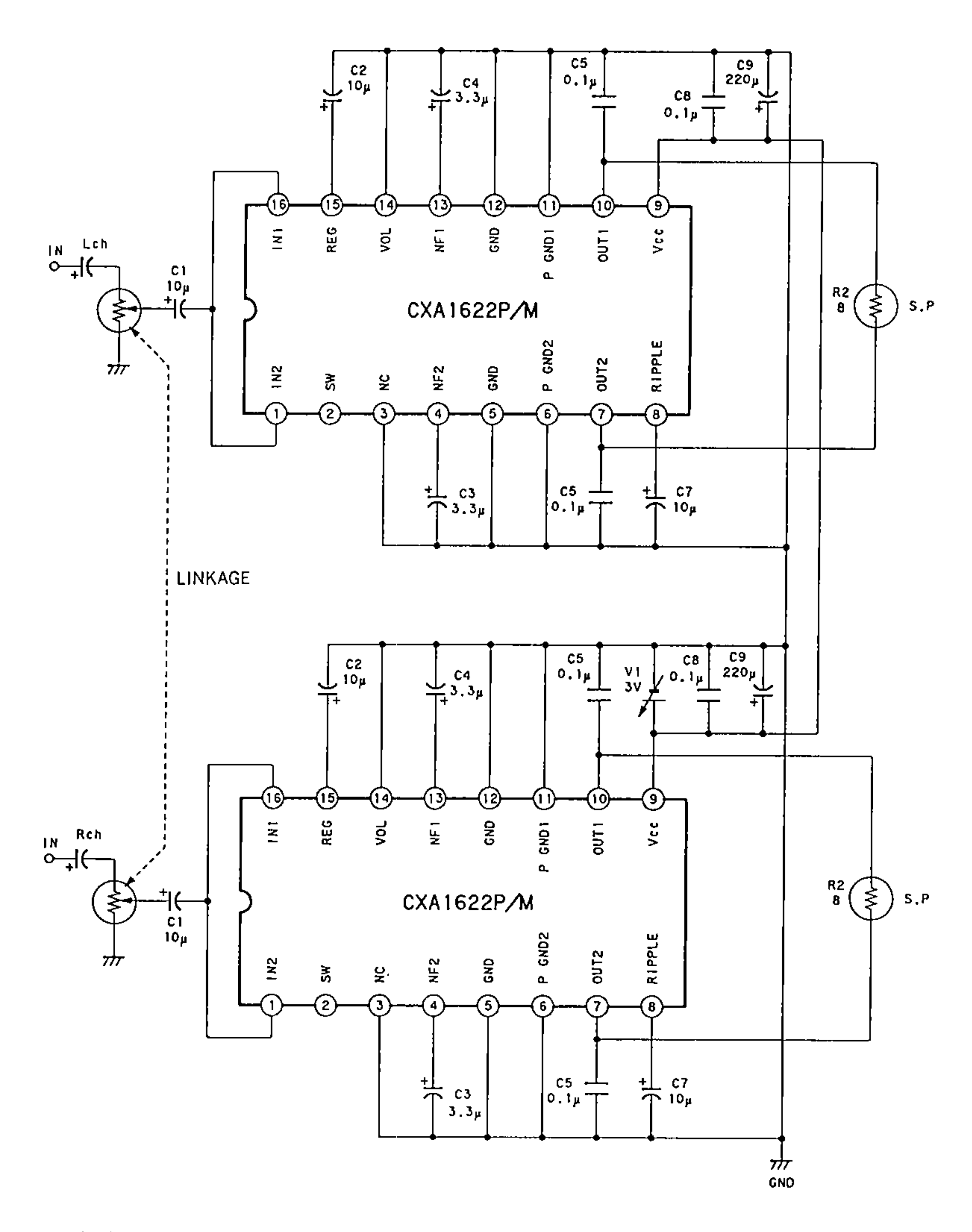
When using internal IC electrical volume



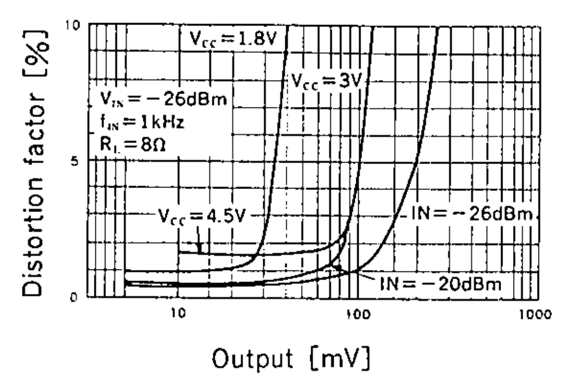
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

BTL, Stereo Application Circuit

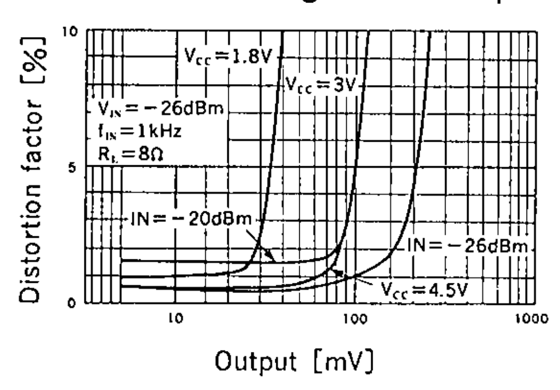
When using IC as fixed gain amplifier



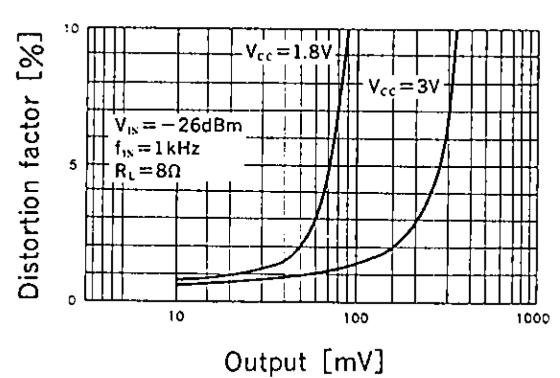
Output vs Distortion 1 A1622P stereo mode single-channel input



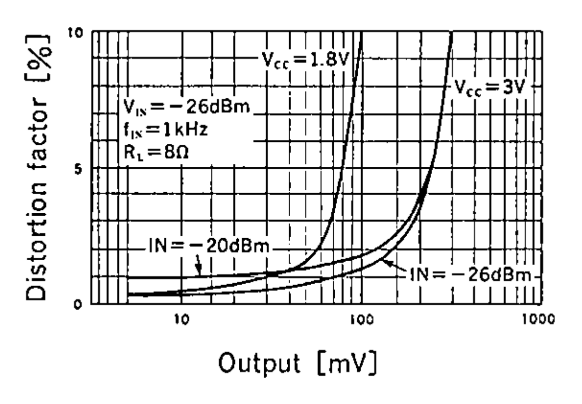
Output vs Distortion factor 2 A1622M stereo mode single-channel input



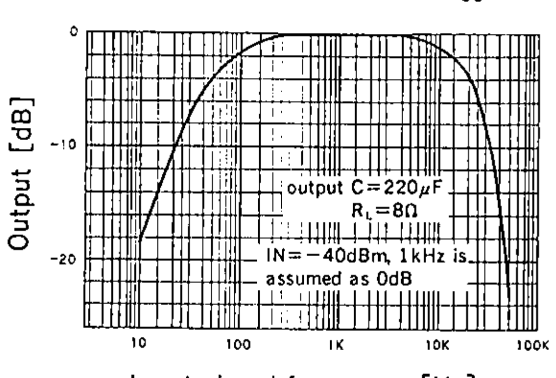
Output vs Distortion factor 3 A1622P BTL mode



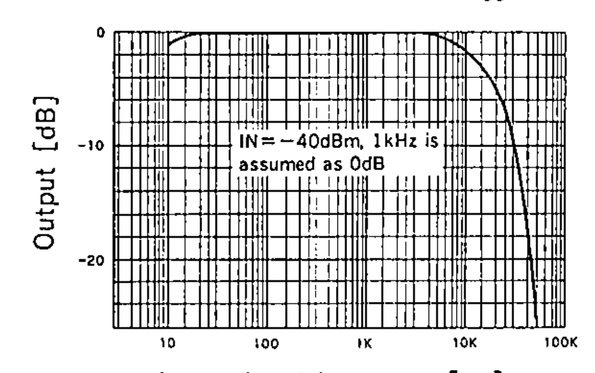
Output vs Distortion 4 A1622M BTL mode



Stereo mode frequency characteristics $V_{IN}=-40dBm$ VOL MAX $V_{CC}=3V$

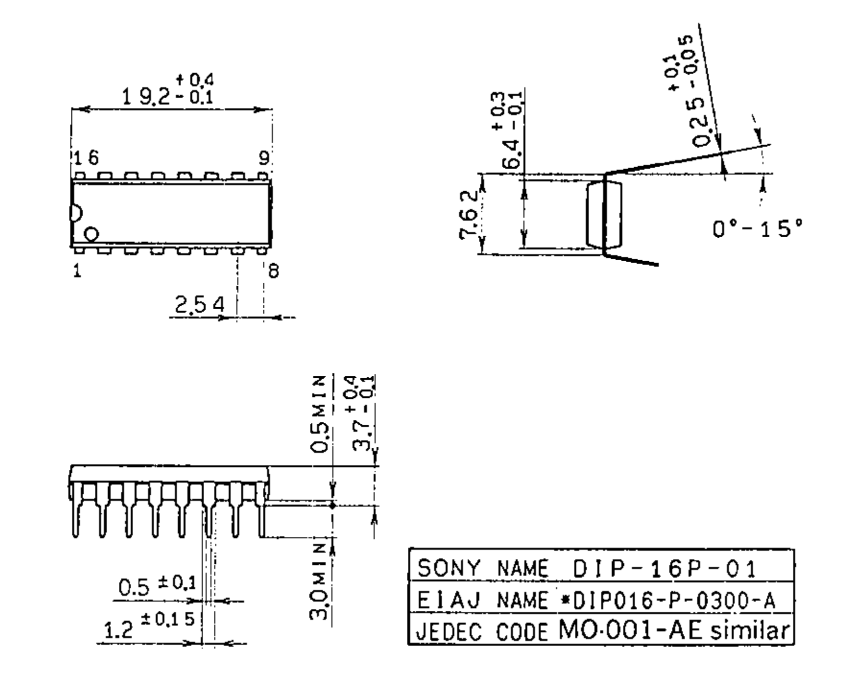


BTL mode frequency characteristics $V_{IN}=-40dBm$ VOL MAX $V_{CC}=3V$



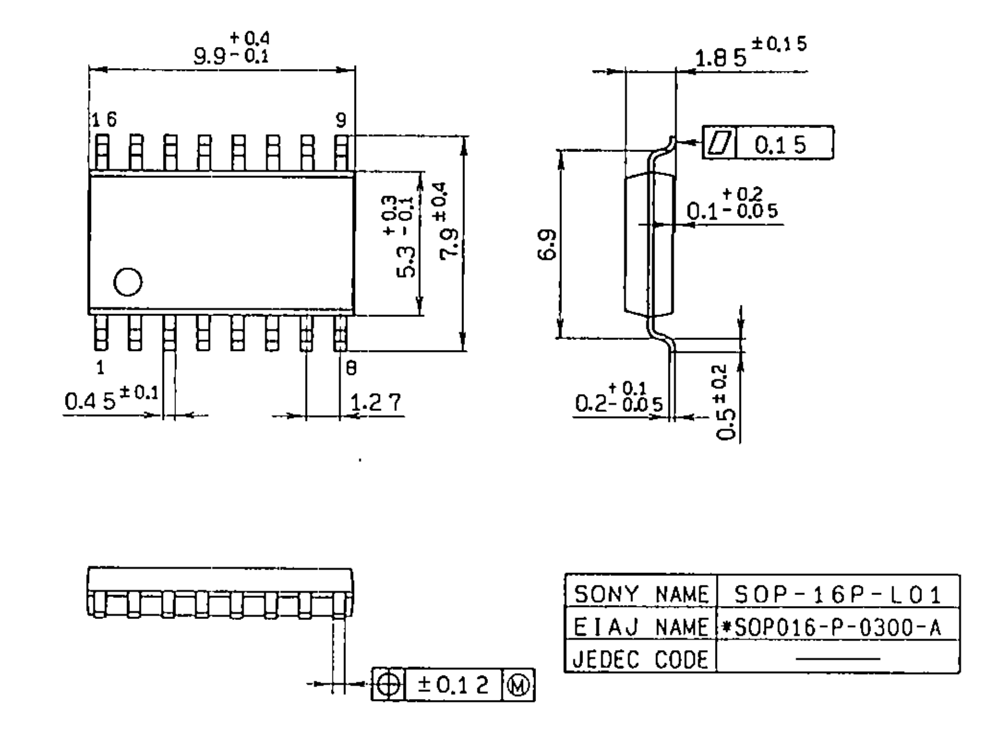
Pckage Outline Unit: mm

CXA1622P 16 pin DIP (Plastic) 300min 1.0g



SONY NAME	DIP-16P-01
EIAJ NAME	*DIP016-P-0300-A
JEDEC CODE	MO-001-AE similar

CXA1622M 16 pin SOP (Plastic) 300mil 0.2g



SONY NAME	SOP-16P-L01
EIAJ NAME	*SOP016-P-0300-A
JEDEC CODE	———